Digital part of SiPM Integrated Read-Out Chip ASIC for ILC hadronic calorimeter

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Abstract

SPIROC is the Silicium Photo-multiplier (SiPM) Integrated Read-Out Chip designed for the future ILC hadronic calorimeter. It reads 36 SiPMs and has an auto-trigger on its 36 channels.

Its main requirements are a 100% trigger rate for signal over 1/2 photoelectron, a charge measurement up to 2000 photoelectrons and a time measurement with an accuracy better than 1ns.

In order to perform all these functions, SPIROC integrates a complex digital part to manage all the different steps of normal working (acquisition, measure and read-out). This ASIC was submitted in June 2007 (technology AMS SiGe 0.35μm).

In this paper, section I describes the general architecture of the ASIC and the main interactions between analogue and digital parts. Section II is dedicated to the different module of the digital part that manages the ASIC.

I. DESCRIPTION OF THE ASIC

A. *Main characteristics*

The SPIROC chip is a 36-channel input front end circuit developed to read out SiPM outputs.

The block diagram of the ASIC is given in Figure 1.

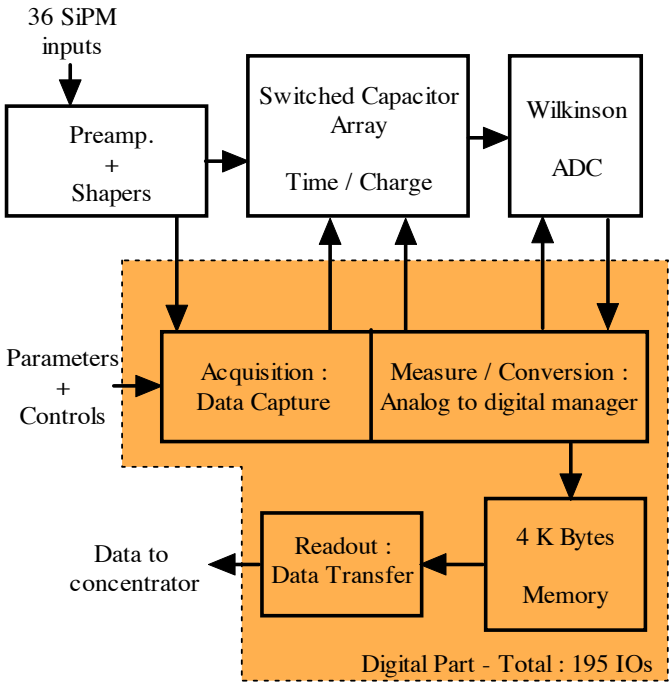

Figure 1: Block diagram of SPIROC

Its main characteristics are given in Table 1.

Table 1: Main characteristics

Technology:	Austria-Micro-Systems (AMS) SiGe 0.35µm
Area:	32mm^2 (7.2mm × 4.2mm)
Power Supply:	5V / 3.5V
Consumption:	25μW per channel in power pulsing mode
Package:	CQFP240 package

For each one of the 36 channels, the PM signal is first amplified thanks to a variable gain preamplifier.

The amplified current then feeds a slow shaper in direct relation with the Switched Capacitor Array (SCA) where analogue voltage will be stored (depth of 16).

In parallel, trigger outputs are obtained via fast channels made of a fast shaper followed by a discriminator. The discriminator output feeds the digital part.

B. *General operation*

The general working of the chip is shown in Figure 2.

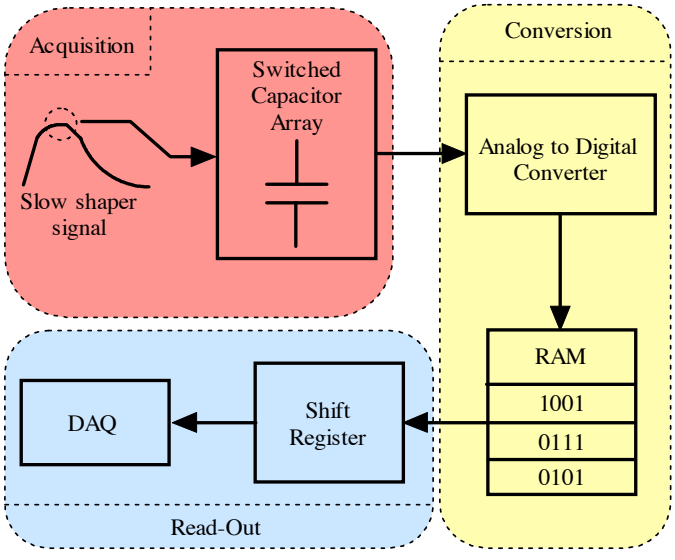

Figure 2: General working

The Acquisition module selects the right column in the SCA to save the analogue value from the slow shaper.

When the SCA is full (depth of 16), the conversion module permits to digitized analogue values from the SCA to digital ones saved in the embedded memory. This is done by managing a 12 bits Wilkinson ADC.

The last module handles the data read out with a serial shift register to the Data Acquisition (DAQ). It also allows to be daisy-chained with other ASICs to minimize lines between boards.

C. *Timing in the future ILC*

The digital part of SPIROC is built around 3 modules which represent the different phases of the ILC operation shown in Figure 3.

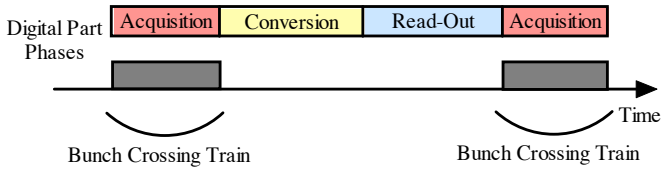

Figure 3: Timing of future ILC

The acquisition module permits to capture data during the bunch crossing train. Conversion and Read-Out ones are activated during inter bunch crossing to convert and save data in the memory in a first step and to read out data in a second one.

Each train is separated by 200ms. The duration of the bunch crossing train is around 1ms.

II. MODULES IN THE DIGITAL PART

A. *Acquisition module*

1) *Block Diagram:*

This module, shown in Figure 4, is dedicated to the SCA management: it selects the column where analogue value should be stored.

It has been developed with asynchronous cells to meet time and low consumption requirements. Besides, this allows no coupling between high speed digital clock (40 MHz not active) and analogue part during acquisition.

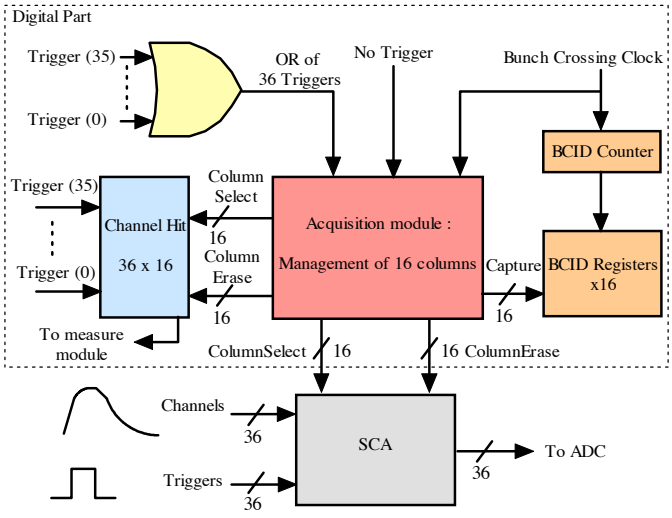

Figure 4: Block diagram of acquisition

2) *Details of operation:*

During idle mode, a capture window is open at the first empty column of SCA (depth 16). When a trigger occurs, data can be captured in this column by means of a "Track & Hold Cell" (T&H Cell) (See Figure 5). When the next bunch crossing occurs, it closes the capture window and selects the next column.

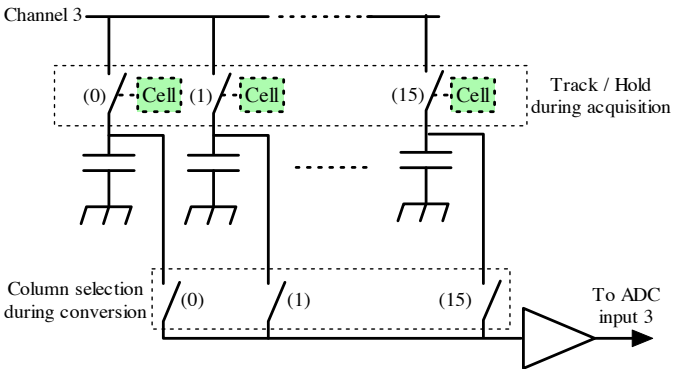

Figure 5: 1 channel of SCA with Track & Hold cell

An external signal is available to erase the active column named "No_Trigger". It can be used to erase the column if a trigger was due to noise.

The Bunch Crossing Identifier (BCID), hit (H) channels and gains (G) are also saved into registers.

For this module, only Slow Clock (Bunch Crossing Clock) is needed.

3) *The T&H cell:*

T&H cell allows to lock the capacitor value only when a calibrated trigger occurs within the selected column.

The hold of the capacitor is made when the trigger disappears.

The selected column is given by the acquisition module and the channel trigger gives the line.

The operation of the asynchronous cell is described below in Figure 6.

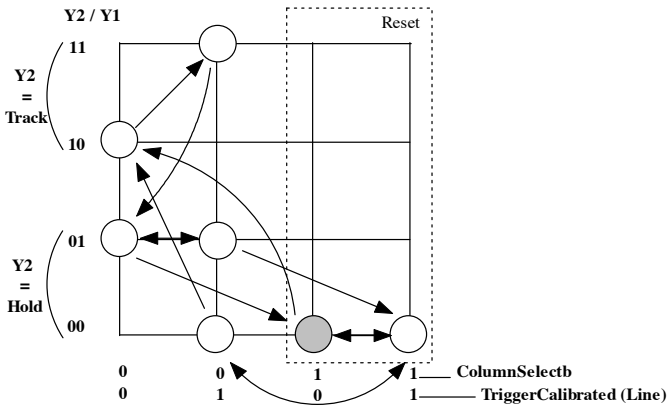

Figure 6: Asynchronous of T&H cell

This operation above is the same as the chronogram in Figure 7.

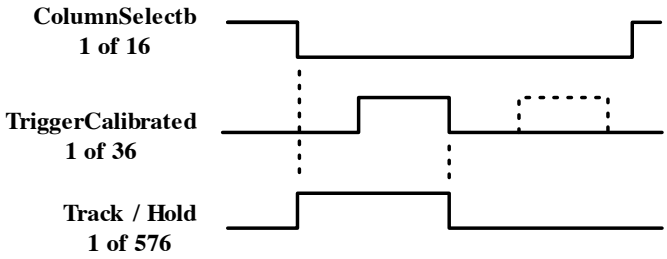

Figure 7: Chronogram of T&H cell

B. Conversion Module

1) Block Diagram:

The main purpose of this module is to convert analogue values stored in the SCA in digital ones.

Figure 8 represents the detailed block diagram of the conversion module.

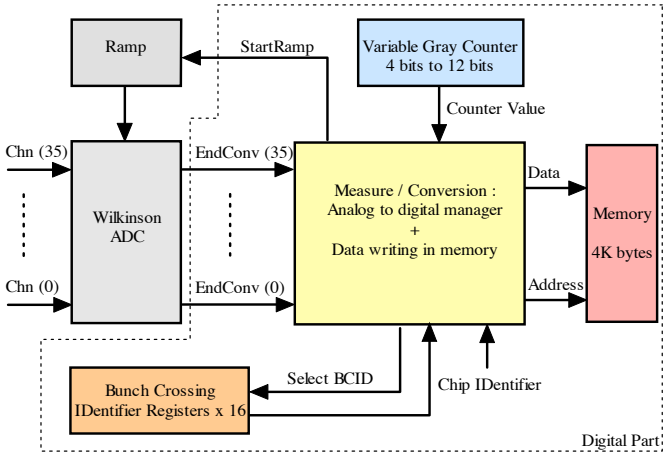

Figure 8: Block diagram of conversion

2) Details of operation:

36 charges and 36 times stored in SCA must be converted for each column. When these 72 conversions are over, data are stored in the memory in order to start a new one for the next column.

The ADC is able to convert 36 analogue values in 1 run (about 100 μs @ 40 MHz). If the SCA is full, 32 runs are needed (16 for charges and 16 for times).

As the default accuracy of 12 bits is not always needed, the number of bits of the counter can be adjusted from 8 to 12 bits.

C. Read-out module

The Readout module permits to empty the memory. To minimize the number of lines between board and external concentrator, data are transferred on a single line.

In the worst case, about 20K bits of data are transferred to the concentrator with a Slow Clock (5 MHz). As the data line to the concentrator is common to all the daisy-chained ASICs, one ASIC can take the data line for a maximum of 4 ms.

Slow Clock and 40 MHz are needed respectively for data and RAM access. The memory mapping is given in Figure 9.

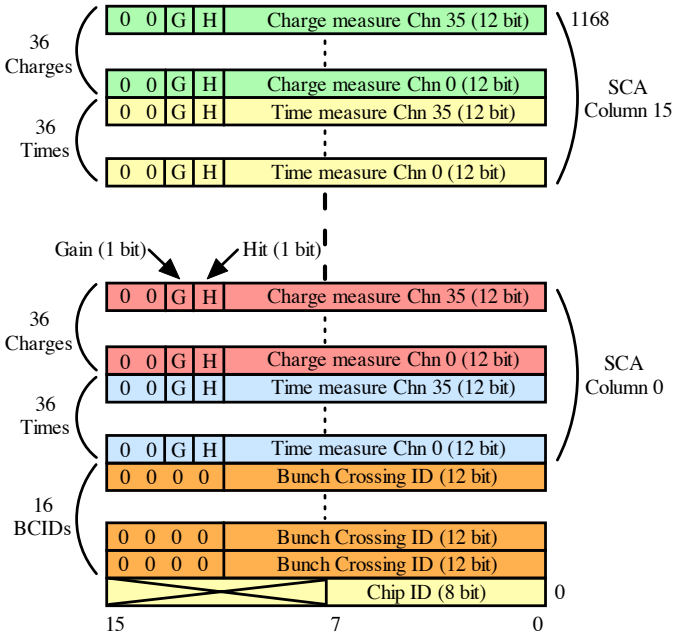

Figure 9: Memory mapping

III. Master Reset of Digital Part

General Reset of the digital part is active low and synchronous with rising edge of Main Clock. It is active for the 2 clock domains (Slow Clock and Main Clock).

To prevent timing violation when Reset is released, it must be synchronised with the 2 clock domains. Reset logic is given below (Figure 10).

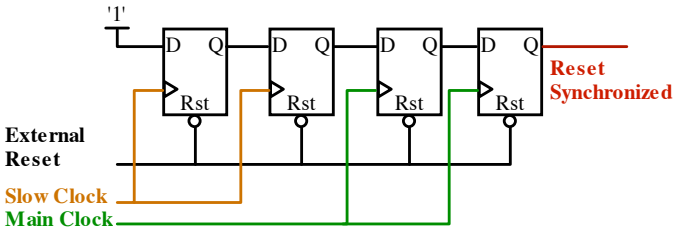

Figure 10: Master Reset logic

This circuit inserts latency when Reset is released (start of digital part). Latency is equal to 2 periods of Slow Clock + 2 periods of Main Clock (450 ns with 5 MHz and 40 MHz). This is shown below in Figure 11.

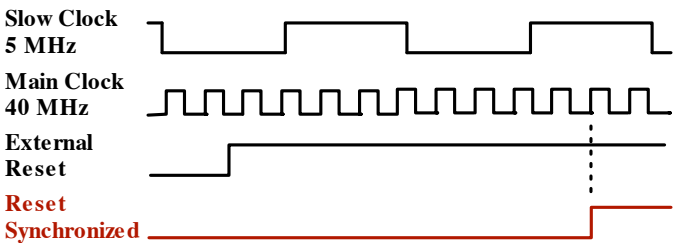

Figure 11: Release of master reset

The Chronogram when reset is set is shown in Figure 12.

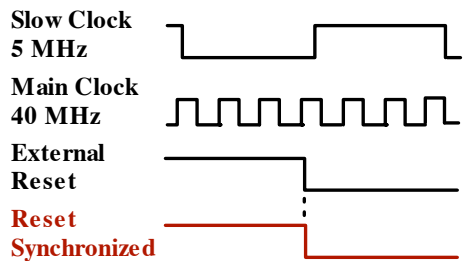

Figure 12: Chronogram of reset activation

IV. Link between DAQ and SPIROC

The 3 modules of the digitals parts are activated by signals from the DAQ. These signals are given in Figure 13.

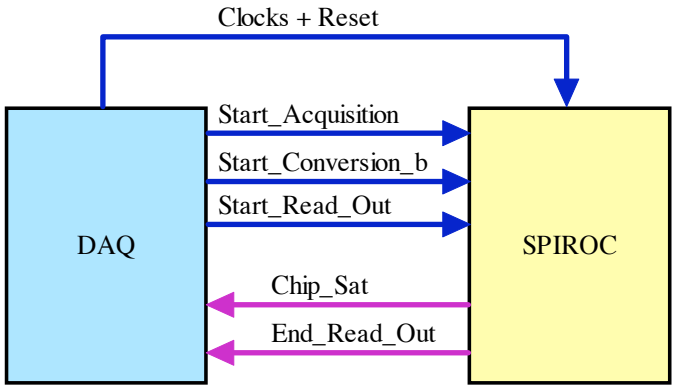

Figure 13: Main Signals between DAQ and SPIROC

The rising edge of the Start_Acquisition signal is the beginning of the acquisition phase for the digital part. The end of the acquisition is given by the falling edge of this signal.

The chronogram of the sequence is given below in Figure 14. In this case, the DAQ stops the acquisition even if the chip is not full (end of bunch crossing for example). The falling edge of Chip_Sat represents the end of the conversion.

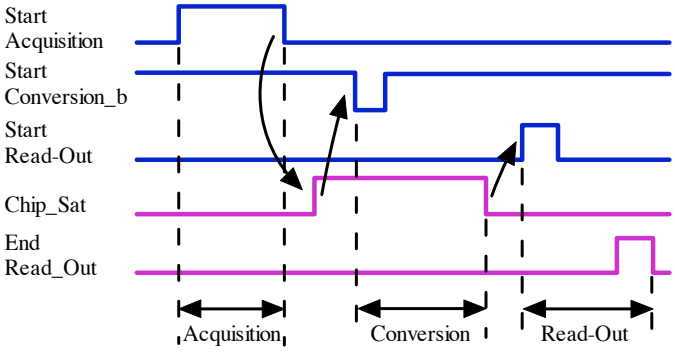

Figure 14: Chronogram with chip not full

Another case is possible when the chip is full during the acquisition phase. This is shown after in Figure 15.

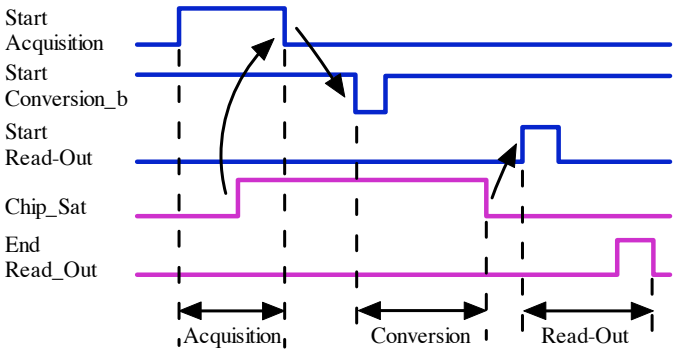

Figure 15: Chronogram with chip full

V. Digital part layout

The layout of the digital part was realized in 0.35 μm technology from AMS and designed with Silicon Ensemble 5.4 from CADENCE (see Figure 16).

The layout is on 3 metals (blue, red and green) and its size is 3000 μm by 1400 μm.

The layout is made around 2 RAMs from AMS.

Each RAM is 2K bytes (2048 words of 8 bits) and 844 μm by 1250 μm.

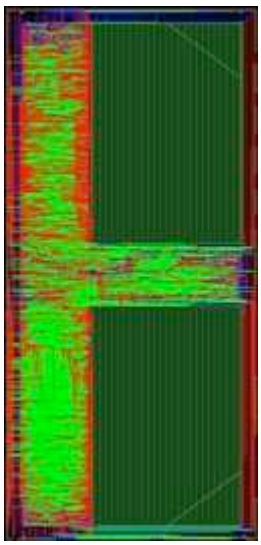

Figure 16: Digital part layout

VI. Conclusion

The digital part of SPIROC includes many functions. Each module has been designed with different constraints: speed optimisation for acquisition, ADC and memory writing management for measurement, line reduction and memory reading for readout.

The ASIC tests will begin in October 2007 and the first results are expected at the end of the year 2007.

Tests of digital part will take a long time due to asynchronous parts and all synchronous state machines to verify.